

A SUPER LOW-NOISE ION-IMPLANTED PLANAR GaAs MESFET MMIC AMPLIFIER

Tetsuro Sawai, Masao Nishida, Toshikazu Hirai, Keiichi Honda,
Tsutomu Yamaguchi, Shigeyuki Murai and Yasoo Harada

Microelectronics Research Center, SANYO Electric Co., Ltd.
1-18-13, Hashiridani, Hirakata, Osaka 573, Japan

ABSTRACT

In order to develop an ultra-compact and super low-noise MMIC amplifier for the receiving system of PHS, the input and output impedance of an ion-implanted planar GaAs MESFET were successfully reduced while maintaining its high-gain and low-noise characteristics. The MMIC had a noise figure of 1 dB and a gain of 13.5 dB at 3 V, 20 mA and 1.9 GHz in an ultra-compact plastic package. The fabricated switch and LNA module employing this MMIC has achieved the low-noise property of less than 3 dB.

INTRODUCTION

Many low-noise amplifier MMICs (LNA-ICs) for mobile communications have been reported to date mainly as a result of a push to reduce the LNA-IC's power consumption [1]. However, as far as we know, no compact LNA-ICs that use GaAs MESFETs to provide a noise figure as low as 1 dB have been found among these reports.

The main reason for this is that it is too difficult to develop a new GaAs MESFET that has low input and output impedance in addition to low-noise and high-gain characteristics. This is because, generally, in LNA-ICs using GaAs MESFETs, the majority of the chip space is taken up by matching circuits, and in L-band LNA-ICs, the occupied area ratio increases due to increasing the input and output impedance of the MESFETs. This increases chip size and makes it difficult to mount it in an ultra-compact package.

We developed an ion-implanted planar GaAs

MESFET that is capable of solving this problem, and realized an ultra-compact high-performance LNA-IC that satisfies the following specifications at 3 V, 20 mA and 1.9 GHz in a plastic package CP6 with a size of 2.9 mm x 1.5 mm.

- (1) Noise figure ≤ 1 dB
- (2) Gain ≥ 13 dB
- (3) Input and output VSWR ≤ 2.5
- (4) Output power 1 dB gain compression ≥ 5 dBm

These specifications were extracted from specifications of our improved switch and LNA module, for PHS (Personal Handy phone System), in which the receiving system is comprised of antenna switches, band pass filters, the above-described IC, and a buffer amplifier (BA-IC) [2] as shown in Figure 1. The module houses control circuits for transmitting and receiving.

Here we report on the LNA-IC employing the developed MESFET and the application to the switch and LNA module.

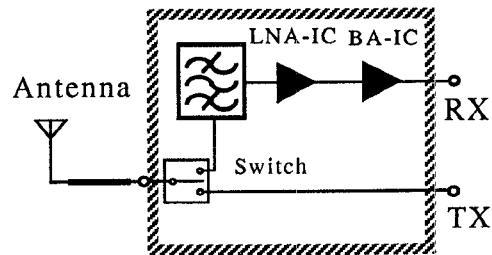


Figure 1 Block diagram of the switch and LNA module

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gain under those ion-implanted conditions (Table 3). Since an IC gain higher than 13 dB was required, we had to have a MESFET MSG of more than 17 dB to account for input and output matching circuit losses and the electrical characteristic fluctuations of the active and passive devices comprising the IC. We found that the gate length and width that complied with the above gain requirement and kept impedance to a minimum were 0.7 μm and 400 μm , respectively. The MESFET fabricated by the above conditions provided a minimum noise figure of less than 0.4 dB at 3 V, 20 mA and 1.9 GHz.

MMIC DESIGN and FABRICATION

We developed the new design methods to use the inductance characteristics of the bonding wire and the lead pin of the compact plastic package as part of the matching circuit. In order to do this, we had to determine individual inductance accurately. The former was done using an equivalent circuit optimization technique and the latter was carried out by obtaining an accurate equivalent circuit, and its parameters for a CP6 package as shown in Figure 3 using our improved electromagnetic field simulation technique [3]. Then to reduce overall IC chip size, we also applied a resonance circuit in the output matching circuit.

We designed and fabricated the LNA-IC in the circuit as shown in Figure 4. The MESFET in the IC features an n+ self-aligned gate structure and buried p-layer structure. To form the Si+ ion-implanted n-layer that plays the key

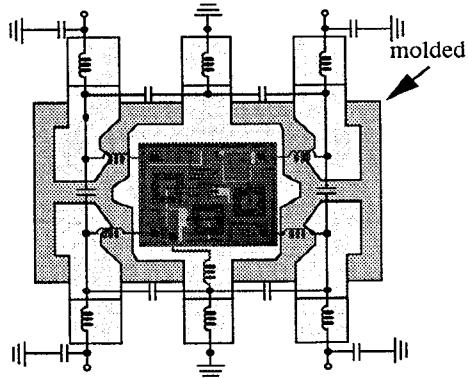


Figure 3 Equivalent circuit of the plastic package (size 1.5 mm x 2.9 mm)

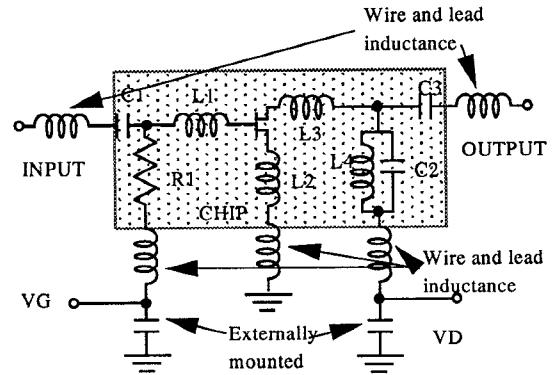


Figure 4 Equivalent circuit of the LNA-IC

role in meeting the MESFET specifications previously described, we used a cap annealing method (temperature: 880°C, time: 5 seconds) with a double-layered SiN film deposited by ECR-PCVD that we originally developed, to achieve a high activation efficiency [4]. Figure 5 shows a photograph of the IC chip. This LNA-IC was fabricated using the MESFET, inductors and MIM capacitances. The line and spacing of the spiral inductor were set to 10 μm and 5 μm , respectively, and the thickness was set to 4 μm in order to reduce parasitic resistance. The chip size was reduced to 0.9 mm x 1.1 mm, which fit into the CP6.

MEASURED RESULTS

Figure 6 shows the noise figure as well as the gain dependence on supply current for the LNA-IC. The characteristics we obtained at 3 V, 20 mA and 1.9 GHz complied easily with the specifications of 1.0 dB for the noise figure and 13.5 dB for gain. By the same token, input and output VSWR were 2.2 and 2.1, respectively. The mea-

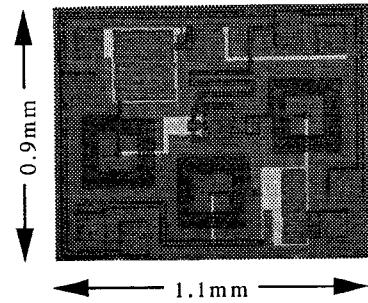


Figure 5 Top view of the LNA-IC chip

Table 1 Correlation between main characteristics and device parameters required to lower MESFET impedance

Device Parameters required to lower impedance	Noise Figure	Gain	Break-down Voltage	Idss
Enlarge gate width	X	X		
Enlarge gate length		X		
Increase doping density of n-implanted layer			X	
Reduce film layer thickness of n-implanted layer				X

X: Marked decline when varied independently

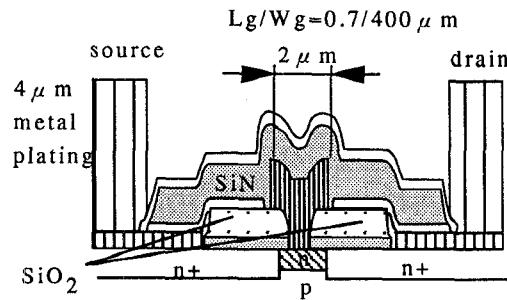


Figure 2 Structure of the GaAs MESFET

DEVICE DESIGN

We developed a new ion-implanted planar GaAs MESFET. In developing the MESFET, the key point was to reduce the input and output impedance as much as possible while maintaining the noise and gain characteristics

Table 2 Ion-implanted n-layer fabrication conditions and measured MESFET characteristics

No.	ion-implanted energy (keV)	Dose X10 ¹² (cm ²)	Impedance (Ω)		MSG (dB)	Idss (mA)	Vbd (-V)
			Input	Output			
			VD=3V ID=20mA, f=1.9GHz		VD =3V	IG =10uA	
(a)	70	3.0	150	250	16.7	28	7 ~ 9
(b)	40	5.2	100	190	16.7	33	6 ~ 8
(c)	30	6.7	110	200	17.0	27	3 ~ 4

so that they conform to specification requirements. There are two basic approaches to accomplishing this.

- (i) Make the doping density and thickness of the implanted n-layer higher and thinner.
- (ii) Enlarge the gate length and width.

As shown in Table 1, however, any attempt to achieve this results in a decline in one or more of the characteristics for noise figure, gain, saturation current Idss and breakdown voltage Vbd, for their respective specification requirements, so we had to achieve optimized levels for each (i) and (ii) .

We began with preliminary experiments related to item (i) using a MESFET having the structure shown in Figure 2. Using a MESFET with a gate length of 0.7 um and a gate width of 400 um, we studied characteristics by varying the implantation conditions of the n-layer as shown in Table 2. The required characteristics were obtained under implant conditions where the ion-implanted energy was 40 keV and the dose was 5.2 x 10¹² cm⁻², but we found that an implant energy of 30 keV resulted in a decline in breakdown voltage, because the dose must be increased to achieve the required operating current. We also found that the input impedance increased by about 50 Ω over that at 40 keV to about 150 Ω at 70 keV. This is why the 40 keV and 5.2 x 10¹² cm⁻² levels mentioned above were used for the ion-implanted n-layer formation.

Then we conducted simulations using gate length and width as parameters in order to determine impedance and

Table 3 Dependence of impedance and MSG on MESFET gate length and width (simulation)
(The conditions for forming n-layer of the MESFET are the same as those shown in No. (b) in Table 2)

Gate Length (um)	Gate Width (um)	Input	Output	MSG (dB)
		Impedance (Ω)	Impedance (Ω)	
0.7	600	65	113	15.9
	400	100	190	16.7
	200	180	350	17.8
1.0	400	90	190	15.8
		115	160	17.2

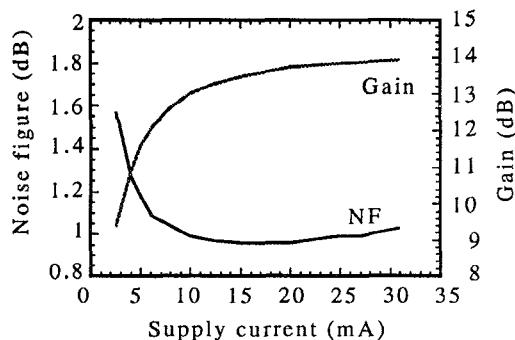


Figure 6 Measured supply current dependence of noise figure and gain of the LNA-IC

sured input and output power characteristics of the IC showed an extremely high output power at the 1 dB gain compression point simular to a 14.5 dBm amplifier.

APPLICATION

We developed a switch and LNA module which required that we combine only capacitors as externally mounted parts, as shown in figure 7. The size of glass-epoxy substrate is 20.6 mm x 7.7 mm. The BA-IC had a noise figure of 2.5 dB and a gain of 13 dB at 3 V, 30mA and 1.9 GHz. The insertion loss of the BPF and PIN switch were 0.6 dB and 1.0 dB, respectively.

Figure 8 shows the noise figure characteristics within 3 dB of the module. The measured values agree with the calculation.

CONCLUSION

An ultra-compact LNA-IC using ion-implanted planar GaAs MESFET with low input and output impedance has achieved the low-noise property of less than 1 dB at 1.9 GHz. We have also developed the switch and LNA module with a noise figure of less than 3 dB employing this LNA-IC.

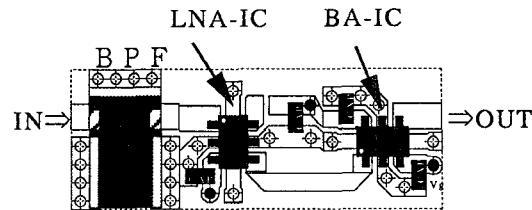


Figure 7 Layout pattern of the LNA module

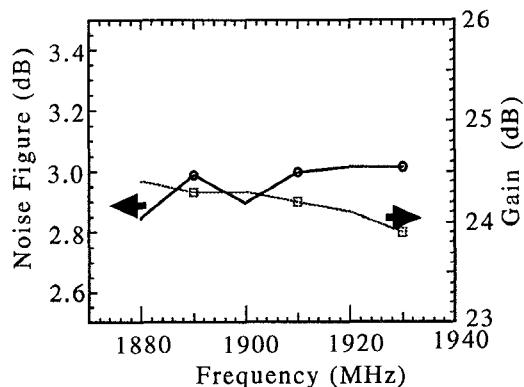


Figure 8 Measured noise figure and gain of the switch and LNA module

REFERENCES

- [1] M. Nakatsugawa et al., "An L-band Ultra Low-Power Consumption Monolithic Low-Noise Amplifier," IEEE GaAs IC Symposium Technical Dig., pp. 45 - 48, 1993.
- [2] S. Murai et al., "A High Power-added Efficiency GaAs Power MESFET and MMIC Operating at a Very Low Drain Bias for Use in Personal Handy Phones," IEICE Transactions on Electronics Vol. E76-C No. 6, June, 1993.
- [3] H. Uda et al., "New Packaging Techniques for Improving Isolation Characteristics of Conventional Plastic Packages for Use in L-band MMIC," Asia-Pacific Microwave Conference Proceedings, Vol. 2 pp. 523 - 526, 1994.
- [4] D. Inoue et al., "Rapid Thermal Annealing of Implanted GaAs Using Double-Layered SiN Films Formed by ECR Plasma CVD," 175th Meeting Electrochem. Soc. State-of-the-Art Program on Compound Semiconductors, 668 SOA, pp. 228C - 229C, 1989